I CLAIM

- 1. Apparatus for processing data, said apparatus comprising:
 - (i) a shifting circuit; and
 - (ii) a bit portion selecting and combining circuit; and
- 5 (iii) an instruction decoder responsive to an instruction to control said shifting circuit and said bit portion selecting and combining circuit to perform an operation upon a data word Rn and a data word Rm, wherein said operation yields a value given by:
- (iv) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn;
 - (v) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction; and
 - (vi) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd.

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- 2. Apparatus as claimed in claim 1, wherein said first portion extends from a most significant bit end of said data word Rn.
- 3. Apparatus as claimed in claim 1, wherein said first portion extends from a least significant bit end of said data word Rn.
 - 4. Apparatus as claimed in claim 1, wherein said shift operand can specify any amount of arithmetic right shift to apply to said data word Rm.
- 25 5. Apparatus as claimed in claim 1, wherein said first portion and said second portion abut within said output data word Rd.
 - 6. Apparatus as claimed in claim 5, wherein said output data word has a bit length of C and C = A + B.

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7. Apparatus as claimed in claim 6, wherein A = B.

- 8. Apparatus as claimed in claim 1, wherein A = 16.
- 9. Apparatus as claimed in claim 1, wherein B = 16.
- 10. Apparatus as claimed in claim 1, wherein said instruction is a single-instruction-multiple-data instruction.
- 11. Apparatus as claimed in claim 1, wherein said instruction combines a data value pack operation with a shift operation.
 - 12. Apparatus as claimed in claim 1, wherein said shifting circuit is upstream of said selecting and combining circuit in a data path of said apparatus.
- 15 13. Apparatus as claimed in claim 12, wherein said selecting and combining circuit is disposed in parallel to an arithmetic circuit within said data path.
 - 14. A method of data processing, said method comprising the steps of decoding and executing an instruction that yields a value given by:
- 20 (i) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn;
 - (ii) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction; and
- (iii) combining said first portion and said second portion to form respectivedifferent bit position portions of an output data word Rd.
 - 15. A computer program product comprising a computer program for controlling a computer to perform a method as claimed in claim 14.

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